CLAIMS

What is claimed is:

1   1.   A method of forming a bipolar transistor, comprising:

2   providing a substrate;

3   forming a first epitaxial layer on the substrate to form a base region having an

4 intrinsic base region and an extrinsic base region;

5   forming an emitter stack on the substrate; and

6   raising the extrinsic base region by forming a second epitaxial layer on the first

7 epitaxial layer.

1   2.   The method of claim 1, wherein the bipolar transistor is a Si, SiGe or

2 SiGe:C npn bipolar transistor.

1   3.   The method of claim 1, wherein the extrinsic base region has a thickness

2 x and the intrinsic base region has a thickness y, and wherein $x > y$.

1   4.   The method of claim 1, wherein the substrate is doped with p-type

2 dopant.

1   5.   The method of claim 1, wherein the first epitaxial layer is a p-type Si,

2 SiGe or SiGe:C layer and the second epitaxial layer is a p-type Si or SiGe layer.

1   6.   The method of claim 1, wherein said forming an emitter stack on the

2 substrate comprises:

3   forming a first oxide layer over the first expitaxial layer;

4   forming a first nitride layer over the first oxide layer; and

5   forming a second oxide layer over the first nitride layer.

1   7.   The method of claim 6, wherein the first oxide layer is a thin silicon

2 dioxide layer, wherein the first nitride layer is a silicon nitride layer, and wherein the

3 second oxide layer is a silicon dioxide layer.

1   8.   The method of claim 6, wherein said forming the first oxide layer

2 comprises thermally oxidizing the first epitaxial layer, wherein said forming the first

3 nitride layer comprises depositing a silicon nitride layer, and wherein said forming the

4 second oxide layer comprises depositing a silicon dioxide layer.

1   9.   The method of claim 6, further comprising:

2   patterning an emitter mask layer over the second oxide layer;

3   selectively etching the second oxide layer and the first nitride layer to form an

4 emitter window; and

5   ion implanting through the emitter window, wherein the ion implant is a self-

6 aligned collector implant.

1   10.   The method of claim 9, further comprising:

2   forming a polysilicon layer on the substrate;

3   etching back the polysilicon layer, wherein the top surface of the polyslicon

4 layer is coplanar with or recessed below the top surface of the second oxide layer; and

5   selectively removing the second oxide layer to expose an emitter polysilicon

6 structure.

1   11.   The method of claim 10, further comprising:

2   forming a second nitride layer on the substrate; and

3   isotropically etching the first nitride layer and the second nitride layer to form a

4 thin nitride spacer.

1   12.   The method of claim 11, wherein said raising the extrinsic base region

2 by forming the second epitaxial layer on the first epitaxial layer further comprises:

3   placing the substrate in a chemical vapor epitaxy device;

4   heating the substrate to a relatively low temperature to minimize diffusion; and

5   introducing silane and diborane or other boron containing gas.

1   13.   The method of claim 12, wherein said raising the extrinsic base region

2 by forming the second epitaxial layer on the first epitaxial layer further comprises:

3   introducing germane with a gradual reduction in germane gas flow to achieve a

4   graded Ge profile in the second epitaxial layer.

1   14.   The method of claim 12, wherein said introducing silane and germane

2   comprises a mole fraction of germane to silane ranging from about 5 to 10 percent.

1   15.   The method of claim 13, wherein said gradually reducing the percentage

2   of germane while depositing the second epitaxial layer comprises reducing the mole

3   fraction of germane from about 5-10 percent to less than 1 percent.

1   16.   The method of claim 11, further comprising:

2   forming a third nitride layer on the substrate; and

3   etching back the third nitride layer to increase the thickness of the thin nitride

4   spacer to form a nitride spacer, wherein the width of the emitter region is increased

5   from f to g when forming the nitride spacer.

1   17.   The method of claim 16, further comprising:

2   forming a silicide layer on the second epitaxial layer and the polysilicon emitter

3   structure;

4   forming an interlayer insulating film on the substrate;

5   patterning and etching the interlayer insulating film to form an emitter contact

6   window, a base contact window, and a collector contact window; and

7   forming an emitter contact, a base contact, and a collector contact.

1   18.   The method of claim 1, wherein said raising the extrinsic base region by

2   forming the second epitaxial layer on the first epitaxial layer further comprises:

3   placing the substrate in a chemical vapor epitaxy device;

4   heating the substrate to a relatively low temperature to minimize diffusion;

5   introducing silane, diborane and, optionally, germane; and

6   gradually reducing the percentage of germane while depositing the second

7   epitaxial layer.

19. The method of claim 1, wherein said heating the substrate to a relatively low temperature comprises heating the substrate to a temperature ranging from 650 to 750 °C.

20. The method of claim 1, wherein said gradually reducing the percentage of germane while depositing the second epitaxial layer comprises reducing the mole fraction of germane from about 5-10 percent to less than 1 percent.

21. The method of claim 1, wherein said forming an emitter stack on the substrate comprises:

forming a first oxide layer over the first expitaxial layer;

forming a first nitride layer over the first oxide layer;

forming a second oxide layer over the first nitride layer;

patterning an emitter mask layer over the second oxide layer;

selectively etching the second oxide layer and the first nitride layer to form an emitter window; and

ion implanting through the emitter window, wherein the ion implanting is a self-aligned collector implant.

22. The method of claim 1, wherein the first epitaxial layer is an SiGe:C epitaxial layer.

23. A bipolar transistor, comprising:

a substrate;

a base region having an intrinsic base region and an extrinsic base;

wherein the extrinsic base region is raised relative to the intrinsic base region;

wherein the extrinsic base region has a thickness x and the intrinsic base region has a thickness y, and wherein $x > y$.

24. The bipolar transistor of claim 23, further comprising an emitter structure, the emitter structure comprising:

a polysilicon emitter having a first portion with a width a, a second portion with a width b, and a third portion with a width c;

5   wherein $c > b > a$; and

6   wherein the first portion defines an emitter base junction, and wherein the third

7   portion defines an emitter contact region.

1   25.   The bipolar transistor of claim 24, wherein the emitter region further

2   comprises a nitride spacer directly adjacent to the polysilicon emitter.

1   26.   The bipolar transistor of claim 23, wherein the extrinsic base region

2   comprises:

3   a first epitaxial layer; and

4   a second epitaxial layer on the first epitaxial layer.

1   27.   The bipolar transistor of claim 26, where the first epitaxial layer is a

2   SiGe epitaxial layer and the second epitaxial layer is a heavily p-type doped Si or SiGe

3   epitaxial layer.

1   28.   The bipolar transistor of claim 23 being an npn transistor.